CHAPTER 5

FLIP-FLOPS

5.0 INTRODUCTION

This chapter will cover "flip-flops." A flip-flop is a digital logic element used for storing binary data. An element capable of storing data is often called a memory or latch. The two kinds of memory encountered in digital electronics are static and dynamic memories. The flip-flop is the basic form of static memory and is also the building block for sequential logic circuits. A primary characteristic of sequential logic circuits is the ability to "remember" the state of the inputs, i.e., memory.

Flip-flops are formed from pairs of logic gates where the gate outputs are fed into one of the inputs of the other gate in the pair. This results in a regenerative circuit having two stable output states (binary one and zero). Frequently additional gates are added for control of the circuit. While some flip-flops are operated asynchronously (without timing pulses), most are operated under clock control in a synchronous system.

Individual flip-flops can be combined to form memory registers, counters and shift registers. A thorough understanding of the basic flip-flop is required for the study of these more complex circuits in later chapters.

5.1 OBJECTIVES

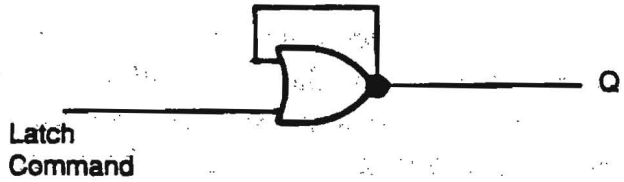
Upon completion of this chapter you should be able to:

- Define and describe the action of a flip-flop.
- Describe and implement a "S-C" (set-clear) flip-flop.
- Describe and implement a "J-K" flip-flop.
- Describe and implement a "D" flip-flop.
- Explain and use a "T" flip-flop.
- Explain the difference between synchronous and asynchronous circuits.
- Describe some common applications of flip-flops.
- Explain what a One-shot is.

5.2 DISCUSSION

In the introduction to this chapter, it was stated that a latch can be made from paired logic gates. While this is true, a simple latch can be formed from a single OR gate. The circuit is constructed by feeding the gate output back into one of the gate inputs as shown in Figure 5-1.

FIGURE 5-1. OR Gate Latch.



When the circuit output is in the LO state and the latch command input is LO the latch will have it's output remain low. When the latch command input is forced HI, the gate output will go HI. The feedback loop from the circuit output to the other gate input will cause the latch to remain in the HI state even when the HI logic level is removed from the latch

command input. The latch is now latched and the command input has no further effect. This circuit is not very practical as the only way to unlatch the output is to remove the power to the gate or to break the feedback connection from the gate's output to the input. Such a latch could be useful under some conditions and is used here to show the basic working of a latch. A similar circuit can be constructed from a pair of NOR gates. The gates are connected as shown in Figure 5-2.

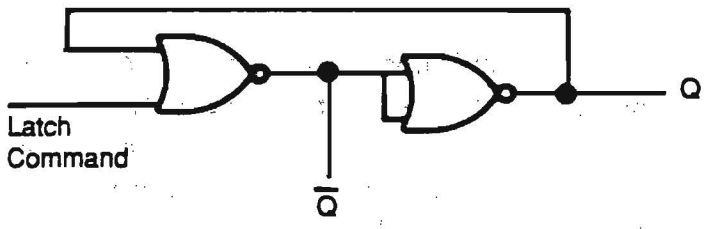


FIGURE 5-2. NOR Gate Latch.

The right most gate in this circuit complements the output ($\overline{Q}$) and the feedback signal to the gate input. The circuit functions the same as the circuit described in Figure 5-1 since complementing the NOR gate output results in the OR function being performed. The advantage of this circuit is that it gives the user access to the complement of the Q output. The circuit shown in Figure 5-2 will take a little more time to latch than the circuit of 5-1 since two gates will have to switch for the circuit to latch. This circuit is still not extremely useful since it is difficult to unlatch the circuit.

5.2.0 Set-Clear Flip-flops

The circuit of Figure 5-2 can be greatly improved by disconnecting one of the inverter stage inputs and using it as the clear input for the latch. This is illustrated in Figure 5-3.

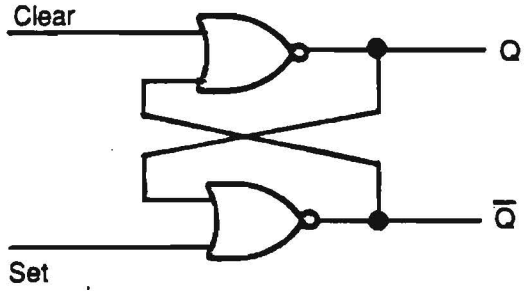


FIGURE 5-3. NOR "S-C" Flip-flop.

The operation of this circuit is straightforward. Assume that initially the Set and Clear inputs and the Q output are all LO. If the Set input is forced HI while the Clear input is forced

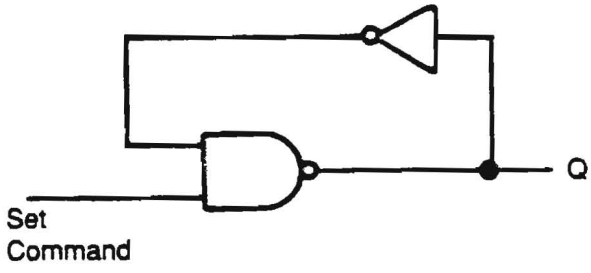
LO, the Q output will be forced to the HI state. The HI Q output causes the complement output to be LO. If the Set line now returns to LO, the Q output will remain HI as long as the Clear input is LO.

The flip-flop can be cleared by bringing the Clear input HI while holding the Set input LO. This results in a LO on the Q output. The LO Q output results in a HI on the complement output. At this point the Clear input can return to the LO state and the flip-flop is cleared until the next Set command is received.

This is all well and good but what if the Clear and Set inputs are brought to the HI state at the same time ? This would result in the true and complement outputs both having to be LO. This state is not allowed since two complement outputs cannot have the same state. The circuit will respond with a race condition with the circuit outputs being LO. For this reason much effort is expended to make certain that the Set and Clear inputs are never both logic one. Additionally, while both inputs can be LO at the same time they cannot reach the LO condition simultaneously without resulting in a race condition with unpredictable circuit outputs. Many refinements to this basic S-C flip-flop were designed to avoid this indeterminate state.

Latches can also be constructed from NAND gates. Figure 5-4 shows a simple NAND latch.

FIGURE 5-4. Basic NAND Latch.



Notice that the latch command input is normally HI and that a LO input is used to Set the latch. A Set-Clear latch can be constructed from NAND gates as shown in Figure 5-5.

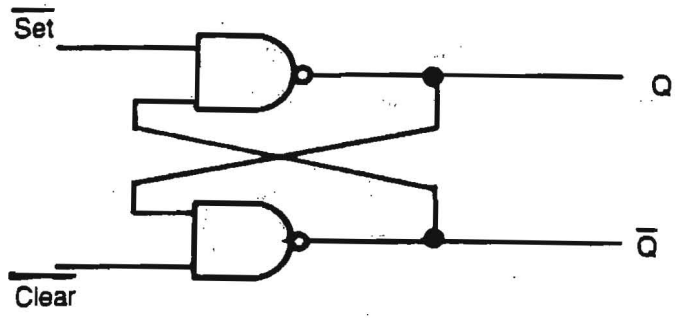


FIGURE 5-5. NAND "S-C" Latch.

The latch performs similarly to the NOR S-C latch except that a LO input is required to activate the Set and Clear inputs. The forbidden state is when S and C are both LO.

5.2.1 The "D" Type Latch

The simple NOR S-C latch can give unreliable and unpredictable outputs if both of the inputs to the latch go to the HI or arrive at the LO state simultaneously. The first case is not allowed and the second case results in a race condition with unpredictable outputs. One way of avoiding both of these circumstances is to provide hardware so that the Set and Clear inputs can never have the same state. This can be accomplished with an inverter as shown in Figure 5-6.

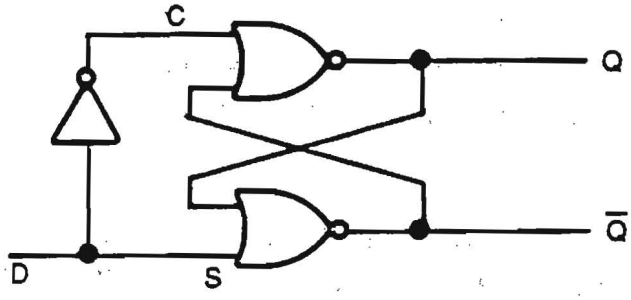
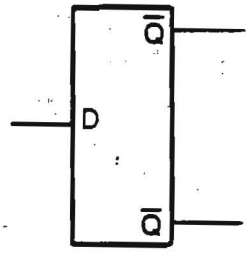


FIGURE 5-6. NOR "D" Latch.

Logic Diagram

Schematic Symbol



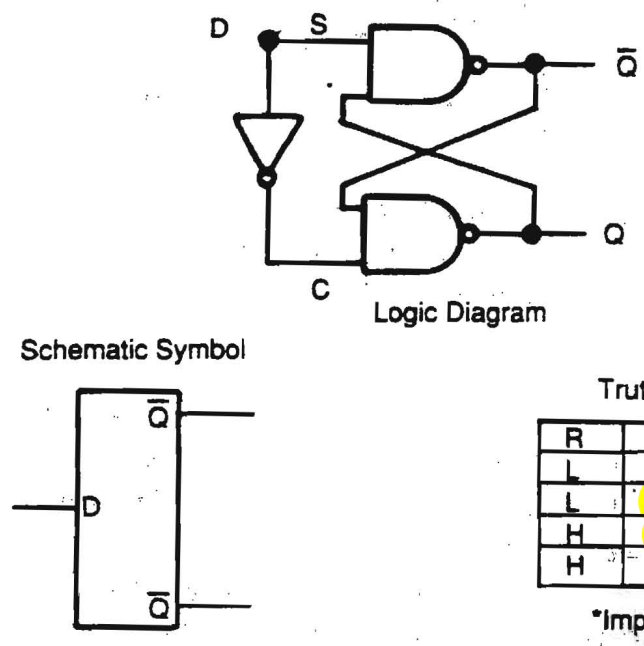
Truth Table

R	S	Q
L	L	*
L	H	H
H	L	L
H	H	*

*Impossible

This circuit is known as a D latch and the circuit input is called the D input. The D latch can also be constructed from NAND gates and inverters as shown in Figure 5-7.

FIGURE 5-7. NAND "D" Latch.



The circuits shown in Figures 5-6 and 5-7 are active HI in that Q goes HI when D goes HI. These latches can be made to perform as active LO circuits by changing which of the inputs to the S-C latch is inverted. The inverter bubble is used to denote the active low D input in schematic diagrams.

5.2.2 Clock Signals

The circuits studied up to this point have been entirely based on combinational logic circuits. This sort of circuit has the state of its output change when the input states change. Circuits of this type are said to operate asynchronously. Asynchronous circuits cannot usefully transfer data to or receive data from other flip-flops.

The ability to be chained (receive and transfer data to other flip-flops) is important for making counter circuits which count the number of pulses received by the circuit. This ability to be chained is also important for constructing registers (small arrays of latches) where inputs can be transferred or shifted from one element of the register to the next. The simple latches studied up to this point cannot be chained because of the inherent

system gate delays and settling time. If we are to transfer states from one flip-flop to another all flip-flops concerned must have completed any previous change and be settled into their present state before a change is attempted. The variable gate delays and settling times between fip-flops prevents this from happening in any extensive circuit particularly when the circuit is operated at high speeds.

Different circuit characteristics result in one of the flip-flops in the chain receiving an input before it is ready and hence one of the states or bits is lost. Another problem that can occur if simple latches are used for counting and shift register circuits is that an input into one end of the directly coupled chain will race through the chain of circuits without stopping. This results in a totally useless circuit.

The solution to these problems is to provide a timing or clock signal that allows all of the flip-flops of the chained circuits to switch simultaneously or synchronously under control of the clock. This means that in clocked circuits the outputs do not change as soon as the inputs change but must wait for a clock signal before the output state can change.

5.2.3 Clocked "S-C" Flip-flops

A clocked S-C flip-flop can be formed by adding two more NAND gates to the simple S-C flip-flop as shown in Figure 5-8.

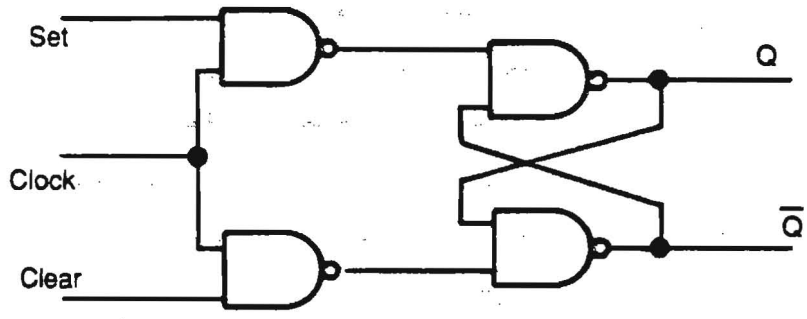


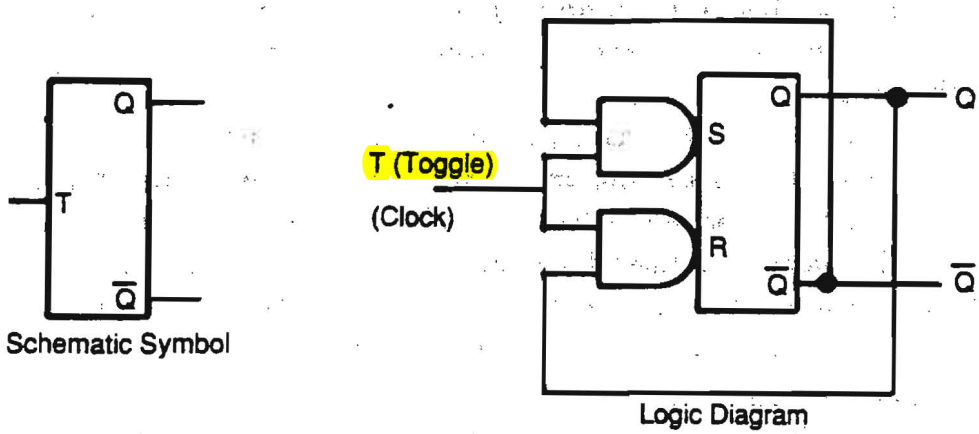
FIGURE 5-8. Clocked "S-C" Flip-flop.

Notice that this circuit only provides clock control of the S-C flip-flop which will still have two sets of conditions which cannot be used in any worthwhile circuit. The Set and Clear inputs are only passed to the main section of the flip-flop when the clock input is HI.

5.2.4 Clocked "T" Flip-flops

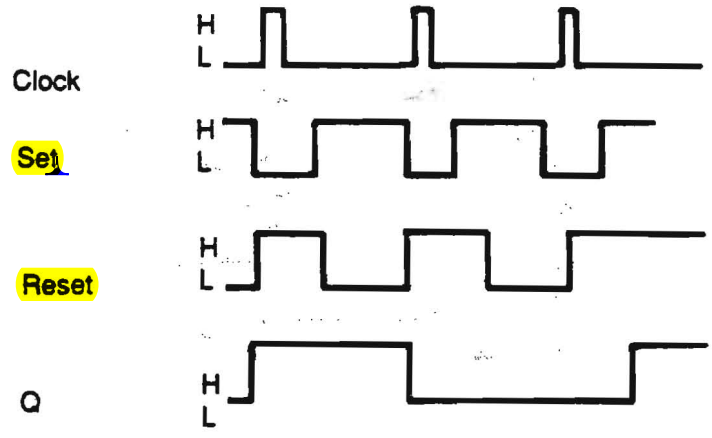
The clocked T flip-flop is a modification of the clocked S-C flip-flop. The true and complement outputs are fed back as shown in Figure 5-9 to act as the Set and Clear inputs.

FIGURE 5-9. Clocked "T" Flip-flop.



When the flip-flop is set the HI Q output is feedback to the reset input. When the next clock pulse occurs, the latch is cleared. The HI Q output is fedback to the set input. When the next clock pulse occurs the latch is set. Note that two clock pulses were needed to change the output state from Set to Clear and back to Set. This type of circuit is called a T flip-flop because of the way the output of the flip-flop toggles or changes to the opposite state with each clock pulse. A timing diagram for the T flip-flop is shown in Figure 5-10.

FIGURE 5-10. Timing Diagram for "T" Flip-flop.

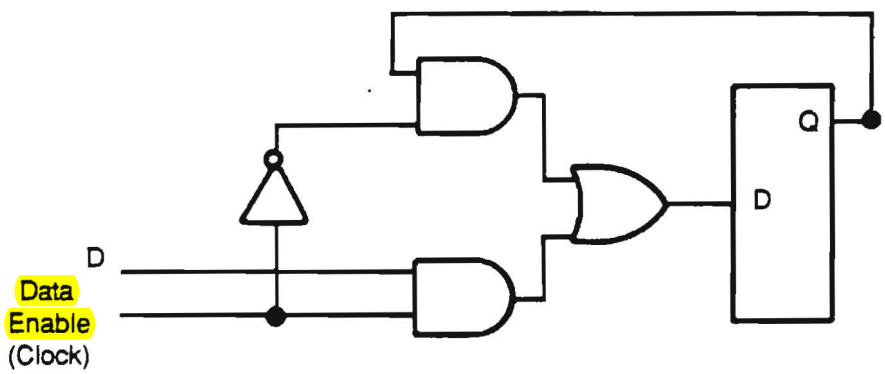


Notice that the frequency of the output signal is one half of the input clock signal frequency. For this reason a circuit of this type is often called a two to one frequency divider. The type T flip-flop is not available as a TTL integrated circuit; however, a circuit of this type is easily constructed from available devices.

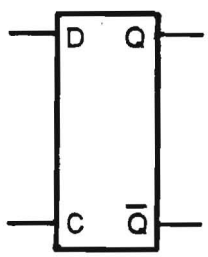
5.2.5 Clocked "D" Flip-flops

We have already studied the D latch. The truth table for the latch shown in Figure 5-7 reveals some interesting qualities of the D latch. Notice that the true output could be replaced with a wire between the D input and the Q output. Similarly, the complement output could be replaced with an inverter between the input and output. The Q output is said to be "transparent" to the D input since the circuit acts as though a wire were connected between D and Q. This circuit is useless as was shown earlier but can be turned into a useful circuit with only a small amount of additional circuitry.

Initially one might be tempted to add an AND gate to the input as was done to the S-C flip-flop to form the clocked S-C flip-flop. This would not work since the input to the D latch would go LO whenever the clock signal went LO regardless of the state of the D input. The circuitry needed to gate the data input into the D latch is shown in Figure 5-11.



Logic Diagram



Schematic Symbol

FIGURE 5-11. Clocked "D" Flip-flop.

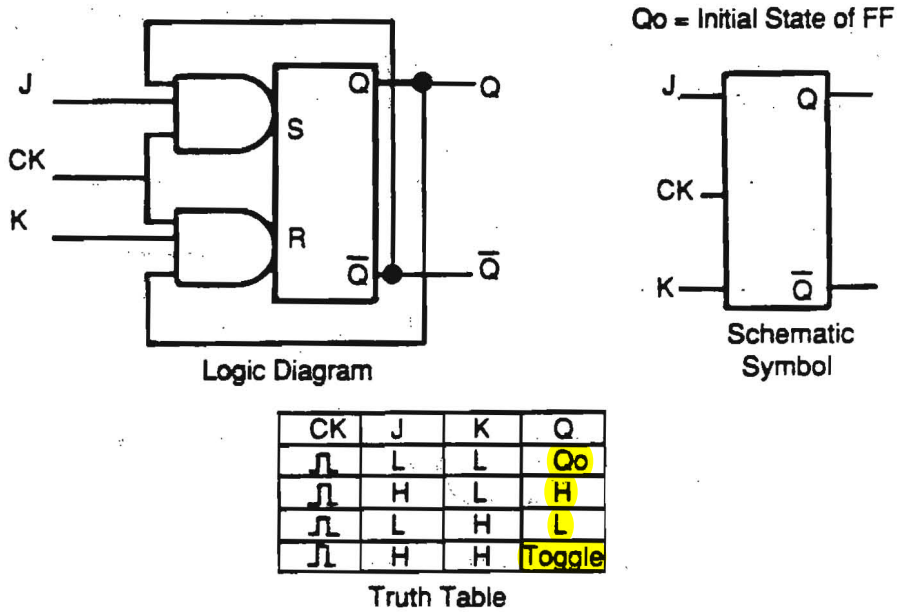
Notice that when the clock signal is HI, the data on the D input is transparent to the Q output. When the clock signal is LO the data on the D input is blocked and the latch stores the output state at the time the clock went LO. The D flip-flop whether clocked or asynchronous is named for it's ability to store data.

D flip-flops are available as edge triggered TTL circuits with Preset and Clear asynchronous inputs that allow setting the initial state of the latch (edge triggered circuits will be explained in the laboratory for this chapter).

5.2.6 "J-K" Flip-flops

The last type of flip-flop you will study is the J-K flip-flop. This type of flip-flop can function as a clocked S-C flip-flop, a clocked D flip-flop, a T flip-flop or can be used to perform other specialized functions. The J-K flip-flop has no ambiguous output states for any input states of the J,K or clock inputs. The J-K flip-flop circuit is shown in Figure 5-12.

FIGURE 5-12. "J-K" Flip-flop.



CK	J	K	Q
⎍	L	L	Qo
⎍	H	L	H
⎍	L	H	L
⎍	H	H	Toggle

Truth Table

The operating characteristics of the J-K flip-flop can be summarized as:

1. J and K inputs LO: when clock goes LO nothing happens.

2. J input HI, K input LO: when the clock goes LO, Q goes or stays HI. $\overline{Q}$ is LO. The HI on the J input is passed directly to the Q output.

3. J input LO, K input HI: when the clock goes LO, Q goes LO and $\overline{Q}$ goes HI. The LO on the J input is passed directly to the Q output.

4. J and K inputs HI: the circuit toggles on each clock pulse. The circuit now behaves like a T flip-flop.

The J-K flip-flop is very flexible and can be used to perform many of the flip-flop functions already studied. The configuration to perform these functions with a J-K flip-flop is shown in Figure 5-13.

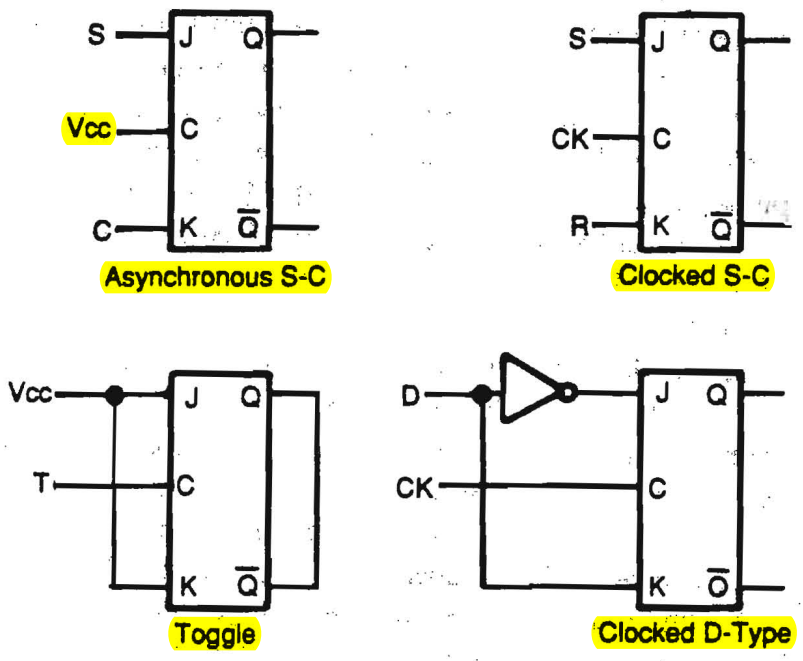


FIGURE 5-13. "J-K" Flip-flop Configurations.

While the J-K flip-flop can perform all of these functions, use of other types of flip-flops may be more economical. The J-K flip-flop is often used in the Master-Slave configuration. In this configuration the state of the flip-flop is determined by the state of the Q output of the Slave flip-flop. The input states to the Slave flip-flop are controlled by the master flip-flop. A circuit diagram for the Master-Slave J-K flip-flop is shown in Figure 5-14.

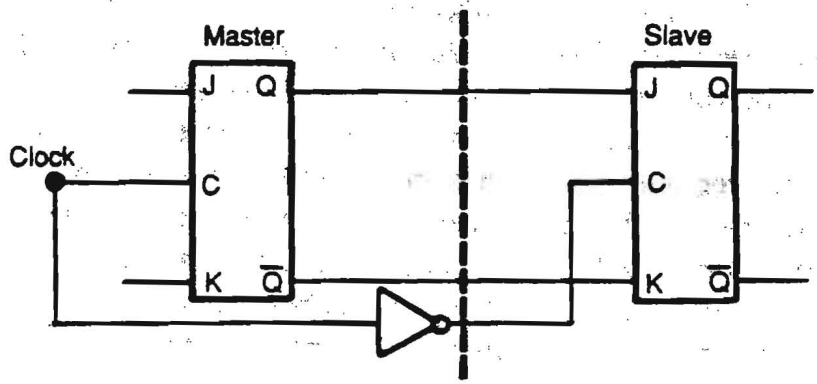


FIGURE 5-14. "J-K" Master-slave Flip-flop Circuit Diagram.

Notice that the J and K inputs determine the state of the Master flip-flop. The clock signal is fed to both sections of the Master-Slave, but is inverted for input to the Slave section.

The operation of this circuit is most readily understood in terms of the clock signal. Assume that the circuit shown is pulse triggered (this only means that we have added no special circuits to cause the circuit to trigger on the edge of the clock pulse). When this is the case, the Master flip-flop will change state to correspond to the state of the J and K inputs when the clock pulse is HI. During this time, the Slave flip-flop will not respond to the outputs from the Master flip-flop because of the inverted clock. When the clock has been HI for a while, the state of the Master flip-flop will be stable and the Slave flip-flop will still be locked out from responding to the outputs of the Master flip-flop. When the clock makes the HI to LO transition, the Master flip-flop will not respond to the J and K inputs since the clock is LO. The inverted clock to the Slave flip-flop will cause the Slave flip-flop to respond to the Q and $\overline{Q}$ outputs of the Master flip-flop. The output of the Slave flip-flop will settle shortly after the falling edge of the input clock pulse.

The Master flip-flop will not respond to the J and K inputs until the next positive going clock transition. The J and K inputs must be stable while the clock is HI for this type of circuit to function correctly.

J-K flip-flops are available as both edge triggered and pulse triggered circuits in the TTL product series. This type of flip-flop is also available with Preset and Clear inputs for setting the initial state of the outputs. These inputs operate asynchronously and cannot be LO simultaneously.

5.2.7 Counting and Frequency Division

Two common applications of J-K flip flops are counting and frequency division. As discussed previously, a J-K flip-flop can be configured to perform as a T flip-flop. This circuit will have an output pulse whose frequency is one-half of the input clock frequency. Any number of these type of flip-flops may be connected with the Q output of the previous stage serving as the clock input to the next stage to provide frequency division by any integer power of two. For instance two flip-flops connected in this manner will have an output frequency equal to one-fourth of the input clock frequency.

A simple counter can be constructed from similar circuits. The J and K outputs are tied HI to form T flip-flops. The Q output of the previous stage is fed to the clock input of the next stage. The Q output also indicates the binary value of the counter. The first Q output has a value of 1, the second a value of 2 , the third a value of 4 and so fourth. A circuit such as this is known as a "binary ripple up-counter." The outputs of all flip-flops must be set to zero before counting is started if an accurate count is to be obtained. Other types of counters will be covered in later chapters.

5.2.8 Monostable Multivibrators

Until now all circuits in this chapter have been flip-flops. Flip-flops are also known as bistable multivibrators. A circuit closely related to the flip-flop is the monostable multivibrator. This is a circuit which has only one stable state. When a trigger pulse is received on the input to the circuit, the output of the monostable multivibrator produces a single output pulse. For this reason, circuits of this type are often called "one- shots."

The duration of the output pulse can be set using external components connected to the pulse length controlling inputs of the one-shot IC. Several types of one-shots are available in the TTL series of ICs. Some have special conditioning circuits on the input to the one-shot to allow slowly changing input pulses to trigger the circuit. Some one-shots are like the one described above which will not respond to additional trigger pulses while the output is in the unstable state.

Retriggerable circuits which will respond to additional trigger inputs while in the unstable state are also available. One-shots are widely used for contact debouncing so that multiple input pulses from a switch are converted to a single output pulse. One-shots are also used to provide pulses of a fixed length from pulse trains composed of varying length pulses.

5.3 SUMMARY

This chapter covered several kinds of latches and flip-flops. You have become familiar with the circuit diagrams for and the operation of six types of common flip-flops. You have seen the difference between asynchronous and synchronous logic circuits and were introduced to clock signals. You have been introduced to the use of flip-flops in frequency division and counting

circuits. The one-shot and some of it's applications were covered.

This chapter forms the foundation for further study of sequential logic circuits in later chapters.

5.4 REVIEW QUESTIONS

1. What is a flip-flop?

2. Draw the circuit diagram and schematic symbol for a S-C flip-flop. Explain the operation of this circuit.

3. Why are clock signals used in sequential logic circuits?

4. What is the primary characteristic of sequential logic circuits?

5. Name six types of flip-flops.

_____ _____

_____ _____

_____ _____

6. What is a name for a flip-flop other than latch?

_____

7. What is a One-shot ?

_____

8. Name an application of One-shots.

_____

9. Name two applications of J-K flip-flops.

_____

_____

10. What is the maximum count that can be contained in a ripple counter made of three J-K flip-flops?

_____

11. Would your answer to question 10 change for "T" flip-flops? Why?

_____

_____

_____